CLAIMS

What is claimed is:

1. A memory control apparatus in a computing system comprising:

a memory controller and a buffer;

said memory controller and buffer being connected by a bidirectional data bus and a control interface;

said buffer being connected to a random-access memory bus for read and write operations;

said buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller;

and a data access and control bus connected between the buffer and the system memory to control read and write operations from and to system memory.

2. The memory control apparatus of claim 1, further comprising:

a second buffer serving as a tag buffer, said second buffer being connected to said random-access memory bus for read and write operations;

said second buffer comprising data storage areas to buffer data between the memory controller and system memory, said buffer further comprising logical circuits to decode memory interface control commands from said memory controller;

and a data access and control bus connected between the tag buffer and the system memory to control read and write operations from and to system memory.

3. The memory control apparatus of claim 2, further comprising:

a tag control input signal designating said second buffer as the tag buffer.

4. The memory control apparatus of claim 3, further comprising:

a memory interface tag bus between the memory controller and the second buffer.

5. The memory control apparatus of claim 1, wherein the control interface between the memory controller and buffer comprises:

a memory interface address bus for transferring memory addresses from the memory controller to the buffer.

6. The memory control apparatus of claim 1, wherein the control interface between the controller and buffer comprises:

a memory interface control bus for transferring memory control commands from the controller to the buffer.

7. The memory control apparatus of claim 1, wherein the buffer comprises:

a read data queue.

8. The memory control apparatus of claim 1, wherein the buffer comprises:

a write data queue.

9. The memory control apparatus of claim 1, wherein the buffer comprises:

a tag data queue.

10. The memory control apparatus of claim 1, wherein the buffer comprises:

control logic for decoding memory interface control commands.

11. The memory control apparatus of claim 1, wherein the buffer comprises:

multiple data and control interfaces to system memory, one to interface with each independent portion of system memory.

12. A method for data transfer between a memory controller and a system memory bus connected to system memory in a computing system comprising:

interposing a buffer between said system memory bus and the memory controller;

providing to said buffer memory interface addresses and memory interface control commands to facilitate said buffer's read and write operations from and to said system memory;

addressing said system memory through said buffer to accomplish read and write operations between the system memory and the memory controller;

decoding in said buffer the memory interface control commands;

temporarily storing data read and write memory data in the buffer during data transfer between the system memory and the buffer; and

transferring read and write memory data between said memory controller and said buffer during read and write operations.

13. The method of claim 12, further comprising:

interposing a second buffer between the controller and system memory serving as a tag buffer.

14. The method of claim 13, further comprising:

updating memory tag information through a tag interface control bus between the memory controller and the tag buffer.

15. The method of claim 12, further comprising:

controlling read and write operations to said system memory with the decoded memory interface control commands originating in the memory controller and decoded in the buffer.

16. The method of claim 12, further comprising:

fanning memory address information received in the buffer from the controller to the system memory through a data address control bus connecting the buffer to the system memory bus.

17. The method of claim 12, further comprising:

interleaving read and write operations in sequences of memory operations between the controller and multiple independent portions of system memory through the buffer.

18. A memory control apparatus in a computing system comprising:

a memory controller and a means for buffering data between said controller and system memory;

said memory controller and buffer means being connected by a bidirectional data bus and a control interface;

said buffer means being connected to multiple random-access memory busses for read and write operations;

said buffer means comprising means for temporarily storing data exchanged between the memory controller and system memory, said buffer means further comprising logical circuits to decode memory interface control commands from said memory controller;

and a data access and control bus connected between the buffer and the multiple random-access memory busses to control read and write operations from and to system memory.